01-31-01 PCT #

526 Rec'd PCT/PTO 29 JAN 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

09/744877

Atty. Dkt. No: 5310-03000

Inventor(s):
Aomar Halimaoui
André Grouillet

Title: PROCESS FOR FORMING AN OXIDE LAYER OF NON-UNIFORM THICKNESS ON THE SURFACE OF A SILICON SUBSTRATE

CERTIFICATE OF EXPRESS MAIL
UNDER 37 C.F.R. §1.10

"Express Mail" mailing label number: EL588984708US
DATE OF DEPOSIT: January 29, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to:
Commissioner for Patents
Box Patent Application
Washington, DC 20231

Derrick Brown

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

INTERNATIONAL APPLICATION NO.: PCT/FR99/01756
INTERNATIONAL FILING DATE: July 19, 1999
PRIORITY DATE CLAIMED: July 28, ~~1999~~ 1998
U.S. APPLICATION NO. (If known):

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. § 371.

2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. § 371.

3. ☐ This is an express request to begin national examination procedures (35 U.S.C. § 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. § 371(b) and PCT Articles 22 and 39(1).

4. ☒ A translation of the International Application into English (35 U.S.C. § 371(c)(2)), including: a title page; 5 page(s) of specification; 1 page(s) of claims 1-7; 1 page(s) of abstract.

5. ☐ Drawings
☐ Formal Figure(s) on sheet(s).

6. ☒ A copy of the International Application as filed (35 U.S.C. § 371(c)(2))
☒ is transmitted herewith (required only if not transmitted by the International Bureau).
☐ has been transmitted by the International Bureau.
☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. § 371(c)(3))
   - ☒ are transmitted herewith (required only if not transmitted by the International Bureau).
   - ☐ have been transmitted by the International Bureau.
   - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. § 371(c)(3)).

9. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
   - ☐ A copy of the Demand for International Preliminary Examination is enclosed.

10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. § 371(c)(4)):
   - ☒ is enclosed.
   - ☐ is not enclosed. Applicant requests the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail. Further, Applicant requests that the NOTICE OF MISSING PARTS-FILING DATE GRANTED be sent to the undersigned representative of Applicant.

11. ☒ Applicant hereby claims priority to:
   - ☒ International Application No.: PCT/FR99/01756 filed July 19, 1999.
   - ☒ France application No.: 98/09607 filed July 28, 1998.

12. ☐ A translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. § 371(c)(5)).

13. ☒ The entire disclosure of the International Application referred to above is considered to be part of the accompanying application and is hereby incorporated by reference herein.

14. ☒ Assignment Papers.
   - ☒ An assignment document is enclosed for recording.
   - ☒ A Recordation Form Cover Sheet in compliance with 37 C.F.R. §§ 3.28 and 3.31 is included.

15. ☒ A Preliminary Amendment.

16. ☐ A substitute specification for pages .

17. ☐ Power of Attorney
   - ☐ Is enclosed.

18. ☐ Information Disclosure Statement (IDS), including:
   - ☐ Form PTO-1449
   - ☐ Reference(s) marked according to Form PTO-1449.

19. ☒ Return Receipt Postcard

20. ☐ Small Entity Status
   - ☐ A small entity statement is enclosed.

21. ☐ Copy of PCT Form PCT/IB/301.

22. ☐ Copy of PCT Form PCT/IB/304.

23. ☐ Copy of PCT Form PCT/IB/308.

24. ☐ Copy of PCT Form PCT/IB/332

25. ☐ Copy of PCT Form PCT/IB/338

26 ☐ Copy of International Request.

27. ☒ Copy of International Preliminary Examination Report.

28. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR § 1.492 (a) (1)-(5): ☐ Neither international preliminary examination fee nor international search fee paid to USPTO and International Search Report not prepared by the EPO or JPO.....$970.00 ☒ International preliminary examination fee not paid to USPTO but International Search Report prepared by the EPO or JPO.....$840.00 ☐ International preliminary examination fee not paid to USPTO but international search fee paid to USPTO.....$760.00 ☐ International preliminary examination fee paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....$670.00 ☐ International preliminary examination fee paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).....$96.00				
ENTER APPROPRIATE BASIC NATIONAL FEE AMOUNT (as selected above):				$840.00
Surcharge of $130.00 for furnishing oath or declaration later than ☐ 20 ☐ 30 Months from the earliest claimed priority date (37 C.F.R. § 1.492(e)).				
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	16 - 20 =	0	x $18.00 =	
Independent claims	3 - 3 =	1	x $80.00 =	
MULTIPLE DEPENDENT CLAIM(S)			+ $260.00 =	
TOTAL OF ABOVE CALCULATIONS:				
Reduction by 50% for Small Entity. A Small Entity Statement must be filed:				
SUBTOTAL:				$840.00
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 Months from the earliest claimed priority date:				
TOTAL NATIONAL FEE:				
Fee for recording the enclosed assignment. The assignment must be accompanied by an appropriate cover sheet. $40.00 per property:				$40.00
TOTAL FEES ENCLOSED:				$880.00

☒ A fee authorization in the amount of $880.00 is enclosed.

☐ Please charge my Deposit Account No. 50-1505/ in the amount of to cover the above fees.

☒ The Commissioner is hereby authorized to charge any other fees which may be required or credit any overpayment to Conley, Rose, & Tayon, P.C., Deposit Account No. 50-1505/5310-03000/EBM.

09/744877

JC07 Rec'd PCT/PTO 29 JAN 2001

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Date January 29, 2001

09/744877

JC07 Rec'd PCT/PTO 29 JAN 2001

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: Unknown
Filed: Herewith
Inventor(s):
Halimaoui, Aomar

Title: PROCESS FOR FORMING AN OXIDE LAYER OF NON-UNIFORM THICKNESS ON THE SURFACE OF A SILICON SUBSTRATE

Examiner: Unknown
Group/Art Unit: Unknown
Atty. Dkt. No: 5310-03000

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Commissioner for Patents
Box Patent Application
Washington, DC 20231

Derrick Brown

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Amendment

Sir:

Please amend the above-captioned application as follows:

In the Specification

On page 1, line 31, please replace the phrase "consists in" with the phrase --includes--.

On page 1, line 34, please replace the phrase "consists in" with the phrase --includes--.

On page 2, line 8, please replace the phrase "consists in" with the phrase --includes--.

On page 2, line 28, please replace the phrase "The subject of the present invention is therefore" with the phrase --Described herein is--.

On page 2, line 33, please replace the phrase "According to the invention, the process is characterized in that it comprises the following steps" with the phrase "The process includes:"

On page 3, line 32, please delete the phrase "of the invention."

After the text on page 5, please add the following paragraph:

--Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made in the elements described herein without departing from the spirit and scope of the invention as described in the following claims.--

In the Claims:

Please amend the claims as follows:

1. A process for forming a silicon oxide layer of non-uniform thickness on a surface of one and the same silicon substrate, [characterized in that it comprises] comprising:

[a) the implantation] implanting in predetermined regions of the substrate [of] an effective dose of atoms of a chemical species which increases the rate of oxidation of the substrate; and

[b) the growth of] growing a silicon oxide layer of non-uniform thickness by [oxidation on] oxidizing the surface of the substrate.

2. (Amended) The process as claimed in claim 1, [characterized in that] wherein the chemical species are chosen from Si, Ge, Ar, Ne and He.

3. (Amended) The process as claimed in claim 1 [or 2, characterized in that the implantation step] wherein implanting in predetermined regions is an ion implantation step.

4. (Amended) The process as claimed in [any one of claims 1 to 3, characterized in that] claim 1 wherein the implantation energy is between 2 and 100 keV[, preferably 2 to 80 keV].

5. (Amended) The process as claimed in [any one of claims 1 to 4, characterized in that] claim 1 wherein the implanted dose is from 5 x 10^{13} to 5 x 10^{15} atoms/cm^2[, preferably 1 x 10^{15} to 5 x 10^{15} atoms/cm^2].

6. (Amended) The process as claimed in [any one of claims 1 to 5, characterized in that] claim 1 wherein growing a silicon oxide layer comprises oxidation [the growth step by oxidation is an oxidation step] in a furnace, by plasma oxidation, electrochemical oxidation or rapid thermal oxidation.

7. (Amended) The process as claimed in claim 6, [characterized in that the step of] wherein growing the silicon oxide layer [is] comprises an oxidation step in a furnace at a temperature of at lest 300°C and in an oxidizing atmosphere.

Please add the following claims:

--8. The process as claimed in claim 2, wherein implanting in predetermined regions is an ion implantation step.--

--9. The process as claimed in claim 1 wherein the implantation energy is between 2 and 80 keV.--

--10. The process as claimed in claim 2 wherein the implantation energy is between 2 and 100 keV.--

--11. The process as claimed in claim 3 wherein the implantation energy is between 2 and 100 keV.--

--12. The process as claimed in claim 1 wherein the implanted dose is from 1×10^{15} to 5×10^{15} atoms/cm^2.--

--13. The process as claimed in claim 2 wherein the implanted dose is from 5×10^{13} to 5×10^{15} atoms/cm^2.--

--14. The process as claimed in claim 3 wherein the implanted dose is from 5×10^{13} to 5×10^{15} atoms/cm^2.--

--15. The process as claimed in claim 4 wherein the implanted dose is from 5 x 10^{13} to 5 x 10^{15} atoms/cm^2.--

--16. The process as claimed in claim 5 wherein the implanted dose is from 5 x 10^{13} to 5 x 10^{15} atoms/cm^2.--

It is believed that no fees are due in connection with the filing of this Preliminary Amendment. However, if any fees are due, the Assistant Commissioner is hereby authorized to deduct said fees from Conley, Rose & Tayon Deposit Account No. 50-1505/5310-03000/EBM.

Respectfully submitted,

Eric B. Meyertons
Reg. No. 34,876

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Date: 1/29/01

The present invention relates in general to a process for forming a silicon oxide layer and more particularly a silicon oxide layer of non-uniform thickness on the surface of a silicon substrate.

In microelectronics, the gate oxide layer, which is a fundamental element of many semiconductor devices such as MOS transistors, is becoming thinner and thinner. Thus, in 0.18 μm technology, thicknesses of less than 4 nm are required for the gate oxide layer. This reduction in thickness of the gate oxide layer necessarily leads to a reduction in the supply voltages of the devices so as to prevent premature degradation of the gate oxide layer. In the case of microprocessors, it is not always possible to reduce the supply voltage, because of the input/output buses (I/O buses) which require higher voltages. To solve this problem, silicon oxide layers of different thicknesses have been grown on predetermined regions of the same silicon substrate, the thickest oxide layers being formed at points where the voltages applied will be the highest.

In order to obtain, on a surface of the same silicon substrate, a silicon oxide layer having two different thicknesses in predetermined regions of the surface of the substrate, a two-step oxidation process has been used.

The first step of the process consists in growing a first layer of silicon oxide of uniform thickness by oxidation on the surface of the substrate.

The second step consists in growing a second silicon oxide layer by oxidation, but with masking of predetermined regions of the surface of the substrate that have already been covered with the first oxide layer, in order in this way to obtain a final oxide

layer of greater thickness in the unmasked regions.

The major drawback of this process is the contamination of the gate oxide during the masking and etching steps.

To remedy the drawbacks of the above masking process, a process has recently been proposed in which a non-uniform thickness oxide layer is grown in a single step. This process consists in forming, on the surface of the substrate, predetermined regions having an oxidation rate reduced by nitrogen ion implantation in these predetermined regions, at points where it is desired to obtain a thinner oxide layer, and then in growing a silicon oxide layer by oxidation of the surface of the silicon substrate. Such a process is described, other others, in the article "Formation of Ultrathin Nitrided SiO_2 Oxides by Direct Nitrogen Implantation into Silicon", by H.R. Soleimani, B.S. Doyle and A. Philipossian, J. Electrochem. Soc., Vol. 142, No. 8, August 1998.

The latter process also has serious drawbacks since the high dose of implanted nitrogen ($>10^{15}$ cm^{-2}) inevitably leads to degradation of the thin gate oxide layer. This drawback is all the more problematic when the implanted regions are in the majority on the substrate and the thinner the oxide layer is thereon (and therefore the more sensitive it is to degradation problems).

The subject of the present invention is therefore a process for growing a silicon oxide layer of non-uniform thickness on a surface of a silicon substrate which remedies the drawbacks of the processes of the prior art.

According to the invention, the process is characterized in that it comprises the following steps:

a) implantation in predetermined regions of the substrate of an effective dose of atoms of a chemical species which increases the rate of oxidation of the substrate; and

b) the growth of a silicon oxide layer of non-uniform thickness by oxidation on the surface of the substrate.

The implantable species which increase the rate of oxidation of a silicon substrate comprise silicon, germanium, argon, neon, helium, phosphorus and arsenic. The preferred species are Si, Ge, Ar, Ne and He and more preferred Si, Ge and Ar.

Although the implantation of phosphorus or arsenic increases the rate of oxidation of a silicon substrate, these species have the drawback, however, of being dopants of silicon which modify its electrical properties, something which is not always desirable.

Increasing the oxidation rate of a silicon substrate obviously depends on the nature of the chemical species implanted, on the implanted dose and on the implantation energy. In general, the dose of chemical species implanted will vary between 5×10^{13} and 5×10^{15} atoms/cm^2, preferably from 1×10^{15} to 5×10^{15} atoms/cm^2.

The implantation energy may vary from less than 2 keV to more than 100 keV, but is generally from 2 to 80 keV and preferably from 2 to 15 keV.

The implantation of atoms of a chemical species into a silicon substrate is conventional and well known in the art. Thus, it is possible to use a process and an apparatus for conventional ion implantation in which the chemical species to be implanted is ionized before being accelerated by means of an electric field.

A conventional apparatus for carrying out such an implantation is the SHC 80-type VARIAN apparatus.

The process of the invention can be used with any type of silicon substrate, whether crystalline, polycrystalline or amorphus.

The step of growing the silicon oxide layer is conventional and may be carried out by oxidation in a standard furnace at a temperature above 300°C and in an oxidizing atmosphere, such as oxygen, diluted oxygen, water vapor, ozone or other gases. It is also possible

to use other conventional oxidation processes such as plasma oxidation, electrochemical oxidation and rapid thermal oxidation (RTO).

EXAMPLE

A silicon oxide layer was grown on silicon wafers by thermal oxidation in a standard furnace (SVG brand) at a temperature of 900°C for 6 minutes in an oxygen atmosphere.

Some of the wafers were subjected beforehand to argon ion implantation in a similar manner but with different implantation energies (VARIAN SHC 80 implantation apparatus).

The thickness of the silicon oxide layers obtained was measured by ellipsometry. The results are given in Table I below.

TABLE I

Implantation energy / Implanted dose	Thickness of the oxide layer formed, nm		
	2 keV	10 keV	80 keV
5×10^{13} at/ cm^2	4.78	5.74	-
5×10^{14} at/ cm^2	5.66	5.92	6.0
1×10^{15} at/ cm^2	6.01	6.75	-
5×10^{16} at/ cm^2	8.8	12.3	11.0

By way of comparison, the thickness of the oxide layer obtained under the same oxidation conditions on a similar silicon wafer that has not undergone oxidation is 4.7 nm.

Ne or He implantation leads to the same results as argon.

Phosphorus and arsenic implantation, with an energy of 10 keV and with implantation does of 2×10^{15} atoms/cm^2 and 3×10^{15} atoms/cm^2 respectively, have led to 12 and 17 nm oxide layers, respectively.

Because the process according to the invention is based on increasing the oxidation rate of a silicon substrate and not on reducing this rate, which is the case in the prior art, the risk of degrading the regions in which the oxide layer is thinnest is eliminated, while at the same time obtaining oxide layers of greater thicknesses suitable for withstanding higher voltages, for example at the I/O buses.

CLAIMS

1. A process for forming a silicon oxide layer of non-uniform thickness on a surface of a silicon substrate, characterized in that it comprises:

a) the implantation in predetermined regions of the substrate of an effective dose of atoms of a chemical species which increases the rate of oxidation of the substrate; and

b) the growth of a silicon oxide layer of non-uniform thickness by oxidation on the surface of the substrate.

2. The process as claimed in claim 1, characterized in that the chemical species are chosen from Si, Ge, Ar, Ne, He, P and As.

3. The process as claimed in claim 1 or 2, characterized in that the implantation step is an ion implantation step.

4. The process as claimed in any one of claims 1 to 3, characterized in that the implantation energy is between 2 and 100 keV, preferably 2 to 80 keV.

5. The process as claimed in any one of claims 1 to 4, characterized in that the implanted dose is from 5×10^{13} to 5×10^{15} atoms/cm^2, preferably 1×10^{15} to 5×10^{15} atoms/cm^2.

6. The process as claimed in any one of claims 1 to 5, characterized in that the growth step by oxidation is an oxidation step in a furnace, by plasma oxidation, electrochemical oxidation or rapid thermal oxidation.

7. The process as claimed in claim 6, characterized in that the step of growing the silicon oxide layer is an oxidation step in a furnace at a temperature of at least 300°C and in an oxidizing atmosphere.

ABSTRACT

The invention concerns a method comprising steps which consist in: a) implanting in predetermined zones of the substrate an efficient dose of atoms of a species accelerating the substrate oxidation kinetics; and b) growing by oxidation a silicon oxide film with non-uniform thickness on the substrate surface. The invention is useful for producing oxide films for MOS transistor grids.

02792

DECLARATION AND POWER OF ATTORNEY
U.S.A.

Attorneys' Docket n°

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name, the information given herein is true, that I believe that I am the original , first and sole inventor (if only one name is listed below), or a first and joint inventor (if plural inventors are named below, or on additional sheets attached hereto) of the subject matter which is claimed and for which patent is sought on the invention entitled : **"Process for forming an oxide layer of non-uniform thickness on the surface of a silicon substrate"**

which is described and claimed in (check one of the following) :

_____ the attached specification;

_____ the specification in application Serial N°_____, Filed_____

X PCT International Application N° **PCT/FR99/01756**, Filed **19 July 1998**

(if application) and was amended under PCT Article 34 on **August 4,2000**

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims , as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefit under Title 35, United States Code , § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having filing date before that of the application on which priority is claimed :

Foreign/PCT Appln. N°	Country	Filing Date	Priority Claimed (Yes / No)
98/09607	France	28 july 1998	Yes

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) or any PCT international application(s) designating the United States listed below and, insofar as the subject matter of each of the claims of this aplplication is not disclosed in the prior United States application or PCT International application in the manner provided by the first paragraph of Title 35, United States Code,§112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations,§1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application :

U.S.Application N°	Filing Date	Status (patented/pending/abandoned)

I hereby revoke any previous Powers of Attorney and appoint Kevin L.Daffer, Reg.No.34,146, B.Noël Kivlin, Reg.No.33,929, Jeff C.Hood,Reg.No.35,198, Eric B.Meyertons,Reg.No.34,876, Joseph P.Lally, Reg.No.38,947, Eric A.Stephenson,Reg.No.38,321, and David A.Rose, Reg. No.26,223, each said attorneys being members or associates of the firm Conley,Rose & Tayon,P.C.as attorney or agent for so long as they remain with such company or firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications as follows :

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true ; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code; and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

==========

1-00 Full name of sole or first inventor : **Aomar HALIMAOUI**

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Signature : _____ **Date :** November 21, 2000

Aomar HALIMAOUI

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Signature : _____ **Date :** November 21, 2000

André GROUILLET